Original Research Paper

Ultra Low Power MUX Based Compressors for Wallace and Dadda Multipliers in Sub-threshold Regime

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Abstract: The computing efficiency of modern column compression multipliers offers a highly efficient solution to the binary multiplication problem and is well suited for VLSI implementations. The various analyses are established more on compressors circuits particularly with Multiplexer (MUX) design. Conventionally, compressors are anatomized into XOR gate and MUX design. In this study, fully MUX based compressors, utilizing the CMOS transmission gate logic have been proposed to optimize the overall Power-Delay-Product (PDP). The proposed compressors are also used in the design and comparative analysis of 4×4-bit and 8×8-bit Wallace and Dadda multipliers operating in sub-threshold regime. The multipliers based on the proposed compressor designs have been simulated using 45 nm CMOS technology at various supply voltages, ranging from 0.3 to 0.5 V. The result shows on an average 89% improvement in the PDP of the proposed compressor blocks, when compared with the existing published results in sub-threshold regime. The multipliers designed using the proposed compressor blocks also show improved results.

Keywords: Sub-Threshold Regime, Compressors, Wallace, Dadda, Han-Carlson Adder

Introduction

In order to maintain the rapid increase of high performance fidelity applications, emphasis will be on incorporation of low power energy efficient modules in future system design. The designs of such modules partially rely on reduced power dissipation in fundamental arithmetic computation units such as adders and multipliers. This motivates us to design energy efficient column compression multipliers by Wallace and Dadda in sub-threshold regime, as few published works are available in this area. The Wallace and Dadda Multipliers consist of three fundamental parts: A partial product reduction module to reduce the partial products matrix to an addition of only two operands, compressors to perform the partial product addition and a final adder part for the final computation of the binary result (Wallace, 1964; Dadda, 1965; Jayaraju *et al*., 2011). Generally, the partial product reduction part of multiplier contributes to maximum power consumption, delay and layout area. Law *et al*. (1999) have been presented a low-power circuit for 16x16-bit Wallace multiplier. In it the 4-2 compressor circuitry, utilizes a non-full-swing pass-transistor carry generator for low power operation. Karuna and Keshab (2001) have been done the exploration of various low power higher order 4-2 and 5-2 compressors units which achieve better performance for both delay and power consumption due to modified XOR and MUX circuits. In paper Chang *et al*. (2004), several designs of 4-2 and 5-2 compressors capable of operating at ultra-low supply voltages range 0.6V to 3.3V have been presented. Here, the XOR-XNOR module eliminates the weak logic on the internal nodes of pass transistors with a pair of feedback PMOS-NMOS transistors.

In paper (Nirlakalla *et al*., 2011), 4-3, 5-3, 6-3 and 7-3 compressors have been used for high-speed multiplication. All the compressors are designed only with half adder and full adders to reduce the vertical critical path more rapidly than conventional compressors. The designed compressors have been

reduced the number of steps required in the bits reduction process which increases speed of the multipliers. In paper (Shen-Fu *et al.*, 1998), a new 3-2 counter and 4-2 compressor has been designed with Double Pass transistor Logic (DPL) to reduce the internal node capacitance on the critical path. The circuits are used to construct the partial-product-summation-tree in the parallel array multiplier. The improvement is achieved in both delay and power performance. In paper (Sreehari *et al.*, 2007), 3-2, 4-2 and 5-2 compressor have been compared with the existing architectures in 0.18 μm CMOS technology. The compressors are analyzed using C

MOS and CMOS + implementations of XOR and the MUX blocks. The architectures perform better over voltage range 0.9 to 3.3 V. In paper (Jorge and Reis, 2012), the architectures of energy efficient 3-2 and 4-2 compressors have been designed using two logic styles, traditional CMOS logic is used for the XOR-XNOR and combination of a traditional CMOS logic with Transmission Gate (TG) logic has been used for MUX. In paper published by (Abdoreza *et al.*, 2013), a 4-2 compressor has been designed by decomposing each XOR gate to three simpler gates among AND/NAND and OR/NOR with the same collective functionality. The results show the superiority of the compressor design in terms of power, delay and PDP. Furthermore, five 54×54-bit binary multipliers based on this 4-2 compressor are faster with 7% less delay and 14% less PDP in comparison to published results. In paper (Menon and Radhakrishnan, 2006), two high-speed 5-2 compressor architectures, designed with XOR–XNOR circuits, which limit the carry propagation delay to a single compressor stage, have been presented. The simulation results of the designs show 25% improvement in speed compared architecture reported in the literature for supply voltages ranging from 1.5 to 3.3 V. In paper published by (Ohsang *et al.*, 2002), a 5-3 compression method has been derived from a fast 2-bit adder cell, which utilizes two XOR gate delays on the critical path and one-stage dynamic CMOS circuit is used for highly customized design. The Multiply And Accumulate (MAC) designed using above 5-3 compressor shows 14.3% speed improvement in terms of XOR delay.

In this study, energy efficient MUX based compressors in sub-threshold regime have been designed. These proposed compressors are used in the design of 4×4-bit and 8×8-bit Wallace and Dadda multipliers. The multipliers comprise of MUX based AND gate array for computing the partial products, MUX based compressors for partial products addition along with MUX based Han-Carlson (HC) adder in the final stage of addition. The use of TG logic in the multiplier designs leads to reduction in PDP and number

of transistors considerably. The proposed 2:1 and 4:1 MUX circuits eliminate the voltage degradations on the internal nodes of TG by adding a buffer at the output node. The simulation results show that the 2:1 and 4:1 MUX based compressor cells and the multiplier architectures function properly at supply voltages, ranging from 0.3 to 0.5 V, at 45 nm technology.

The rest of the paper organization is as follows-- Section 2, describes the circuit implementation of compressor cells, 2:1 MUX, 4:1 MUX, XOR gate and gate and 2-2, 3-2, 4-2, 5-2, 6-2 and 7-2 compressors in detail with focus on their energy efficiency. Section 3, gives the simulation results of all the basic modules of the compressors. In section 4, the implementations of 4×4 and 8×8 bit Wallace and Dadda multipliers have been done using the proposed compressor cells. Section 5 describes the simulation methodology and overall experimental results of multipliers. All the proposed compressor cells and multipliers are characterized in terms of power, delay and Power Delay Product (PDP). Finally, section 6 presents a summary of the paper and the concluding remarks.

Basic Modules of Compressor and their Circuit Implementations

Conventionally, the implementations of compressors are composed of serially connected full adders and MUX. At gate level, high input compressors are anatomized into XOR gates and carry generators are normally implemented by MUXs. Therefore, different designs can be classified based on the critical path delay, in terms of the number of primitive gates. There are several designs of the XOR and MUXs presented using different logic styles by (Sreehari *et al.*, 2007; Zimmermann and Fichtner, 1997). All the basic modules of compressors with TG logic have implemented at 45 nm technology for sub-threshold operation.

MUX Vs. XOR

Multiplexers (the function of selecting the input from one of 'n' sources to its one output line) are used as one method of reducing the density of integrated circuit packages required by a particular digital circuit design. This in turn reduces the cost of the system. The TG designs 2:1 MUX, 4:1 MUX and XOR gate implementations are shown in Fig. 1-3. The channel length for all transistors is fixed at 50 nm.

The modified TG based 2:1 and 4:1 Multiplexers module eliminate the voltage degradations on the internal nodes of TG by adding a buffer at the output node. The designed circuit quickly isolates multiple signals with a minimal investment in board area and with a negligible degradation in the characteristics of

those critical signals. This design provides true bi-directional connectivity without degradation of the input signal. The output buffer formed by the cascaded inverters is designed in such a way that the first inverter is half the size of the output inverter in order to cut down the power dissipation.
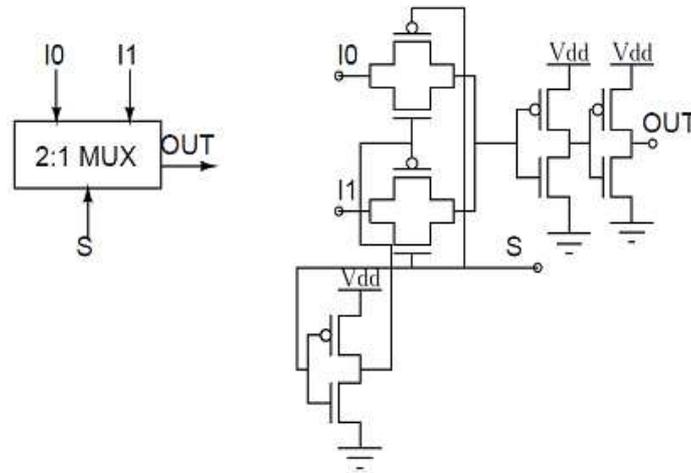
Fig. 1. 2:1 MUX using TG logic
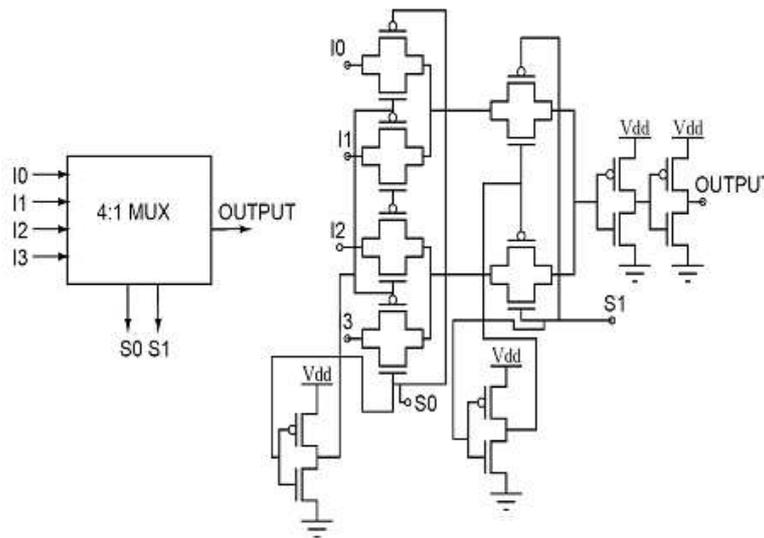
Fig. 2. 4:1 MUX using TG logic
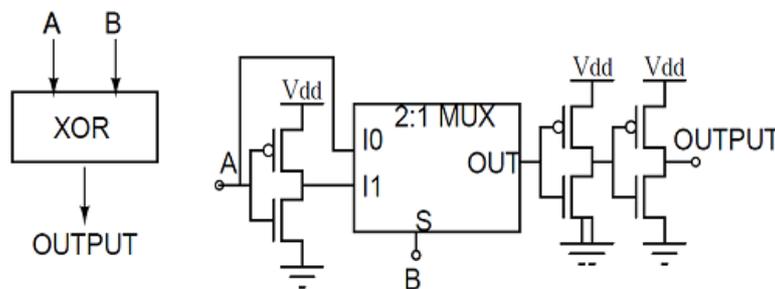
Fig. 3. Proposed XOR gate module
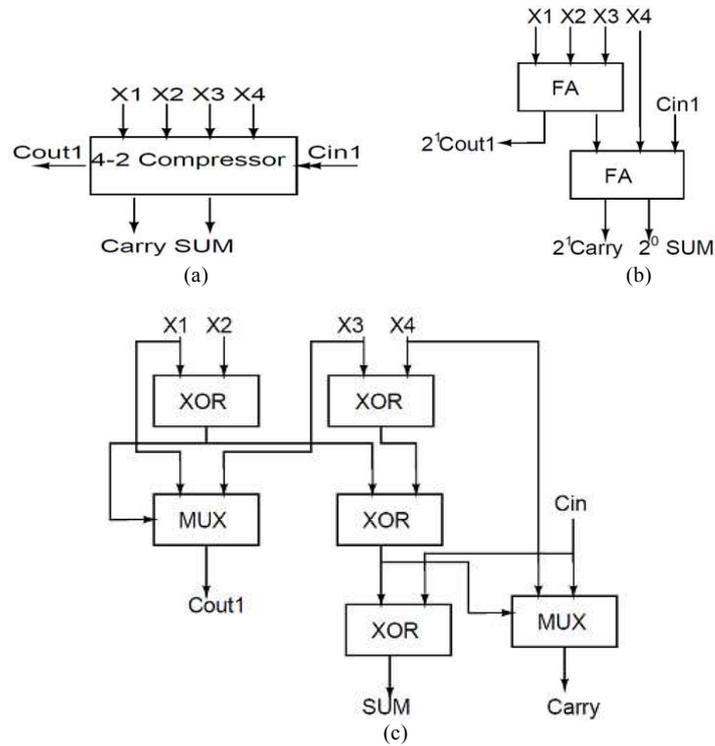
Fig. 4. The conventional architecture of 4-2 compressors
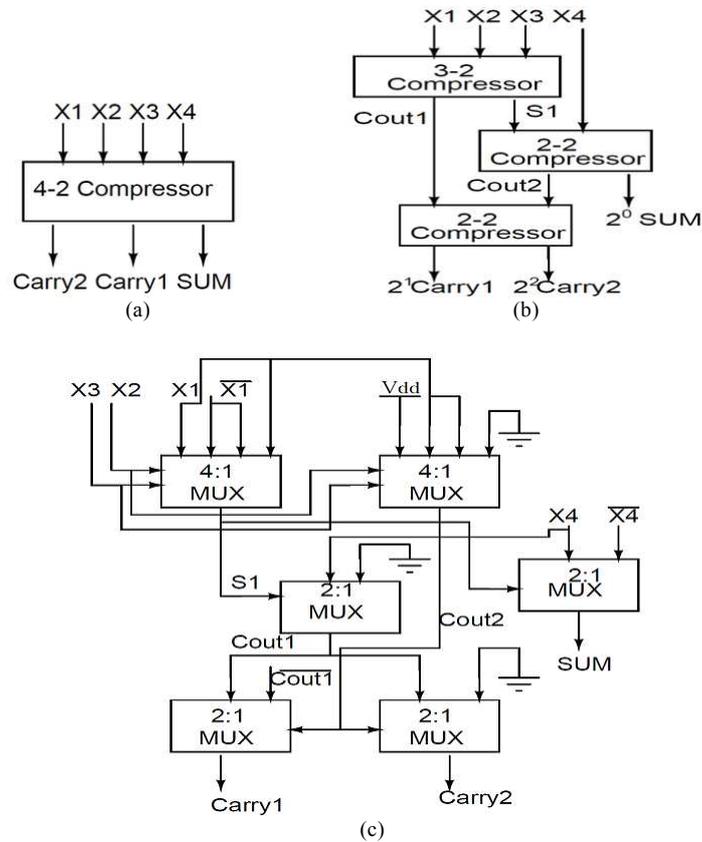
Fig. 5. The proposed architecture of 4-2 compressors

Compressor

The compressors are the bit-compressing cells with principal application in multi-operand addition and multiplication hardware. Therefore, performance of the compressors decides the efficiency of multiplication intensive computations. A 4-2 compressor cell can be implemented in many different logic structures. However, in general, it comprises of three main modules, the first module is required to generate XOR/XNOR function, the second module is used to generate sum and the last module is used to produce the carry output. Figure 4 shows the conventional and proposed architectures of a sample 4-2 compressor.

Conventional and proposed 4-2 compressor is shown in Fig. 4 and 5 respectively, where '4' is the number of input bits. The four numbers of inputs (X0, X1, X2 and X3) and the output SUM have the same weight as shown in Fig. 4a. The output Carry is weighted one binary bit order higher and 4-2 compressor receives an input Cin1 from the preceding module of one binary bit order lower in significance. It produces an output Cout1 to the next compressor module of higher significance as shown in Fig. 4b. At the gate level, high input compressors are anatomized into XOR gates and carry generators are normally implemented using multiplexers as shown in Fig. 4c.

In Fig. 5a, the proposed 4-2 compressor has four inputs (X0, X1, X2 and X3) and outputs (SUM, Carry0, Carry1). In contrast to the conventional design, the proposed 4-2 compressor is composed of one 3-2 compressor and two 2-2 compressors shown in Fig 5b. In the proposed 4-2 compressor, there is no Cin input received from the adjacent compressor. The 3-2 and 2-2 compressors are anatomized into multiplexers only, which in turn are implemented using TG family as shown in Fig. 5c.

The conventional and proposed 4-2 bit compressor abides by the fundamental equation as given in Equation 1 and 2:

$$X0 + X1 + X2 + X3 + Cin1 = 2^0 SUM + 2^1.(Carry + Cout1) \quad (1)$$

$$X0 + X1 + X2 + X3 = 2^0 SUM + 2^1 Carry1 + 2^2 Carry2 \quad (2)$$

Designs of Lower and Higher Level Compressors

In the study compressors are divided into two parts, the first is the lower level compressors that employ 2-2 and 3-2 compressors and the second is the higher-level compressors, which employ 4-2, 5-2, 6-2 and 7-2 compressors. Higher-level compressors can be derived using a single bit adder circuit. It has four/five/six/seven inputs and three outputs and these are made by using the lower level compressors. Input combinations and the corresponding decimal counts of all the proposed compressors and their functionalities are shown in Table1.

Lower Level 2-2 and 3-2 Compressors

The 2-2 and 3-2 compressors are widely used building blocks for high precision, energy efficient column compression multipliers. A 3-2 compressor can also be employed as a full adder cell which takes three inputs, X1, X2, X3 and generates two outputs Sum 'S' and Carry 'C'. A 2-2 compressor acts as a half-adder cell, takes two inputs X1, X2 and generates two outputs Sum 'S' and Carry 'C'. The proposed modified energy efficient compressors have been implemented using TG based 2:1 and 4:1 MUX in sub-threshold regime, as shown in Fig. 6. In order to demonstrate the efficiency of the new designs, we have analyzed the power consumption and other general characteristics of the 2-2 and 3-2 compressor designs against several published low power compressors. The channel length for all transistors is fixed at 50 nm.

The proposed compressors operate on sub-threshold conduction currents to perform circuit operations and give an overall PDP improvement as compared to traditional compressors.

Higher Level 4-2, 5-2, 6-2 and 7-2 Compressors

The proposed compressors utilize the standard hierarchical design approach, where the higher-level compressors are built using lower level compressors. In the proposed higher-level compressors, the carry propagation remains within the block, which simplifies the design. The internal output carries (Cout1, Cout2 and Cout3) from one of the internal blocks acts as the carry input to another block and finally generates one SUM and two carry (Carry1, Carry2) outputs as shown in Fig. 7.

Table 1. Truth table of compressors

(Decimal count)	Input conditions	2-2 outputs (C,S)	3-2 outputs (C,S)	4-2 outputs (C2,C1,S)	5-2 outputs (C2,C1,S)	6-2 outputs (C2,C1,S)	7-2 outputs (C2,C1,S)
0	All the inputs are zero	(0,0)	(0,0)	(0,0,0)	(0,0,0)	(0,0,0)	(0,0,0)
1	Any one input is one	(0,1)	(0,1)	(0,0,1)	(0,0,1)	(0,0,1)	(0,0,1)
2	Any two inputs are one	---	(1,0)	(0,1,0)	(0,1,0)	(0,1,0)	(0,1,0)
3	Any three inputs are one	---	---	(0,1,1)	(0,1,1)	(0,1,1)	(0,1,1)
4	Any four inputs are one	---	---	---	(1,0,0)	(1,0,0)	(1,0,0)
5	Any five inputs are one	---	---	---	---	(1,0,1)	(1,0,1)
6	Any six inputs are one	---	---	---	---	---	(1,1,0)
7	All the inputs are one	(1,0)	(1,1)	(1,0,0)	(1,0,1)	(1,1,0)	(1,1,1)

Note: C, C1, C2 are the carry bits, S is the Sum bit of compressors. C2 is the most significant bit and S is the least significant bit

Fig. 6. Proposed designs of 2-2 and 3-2 compressors
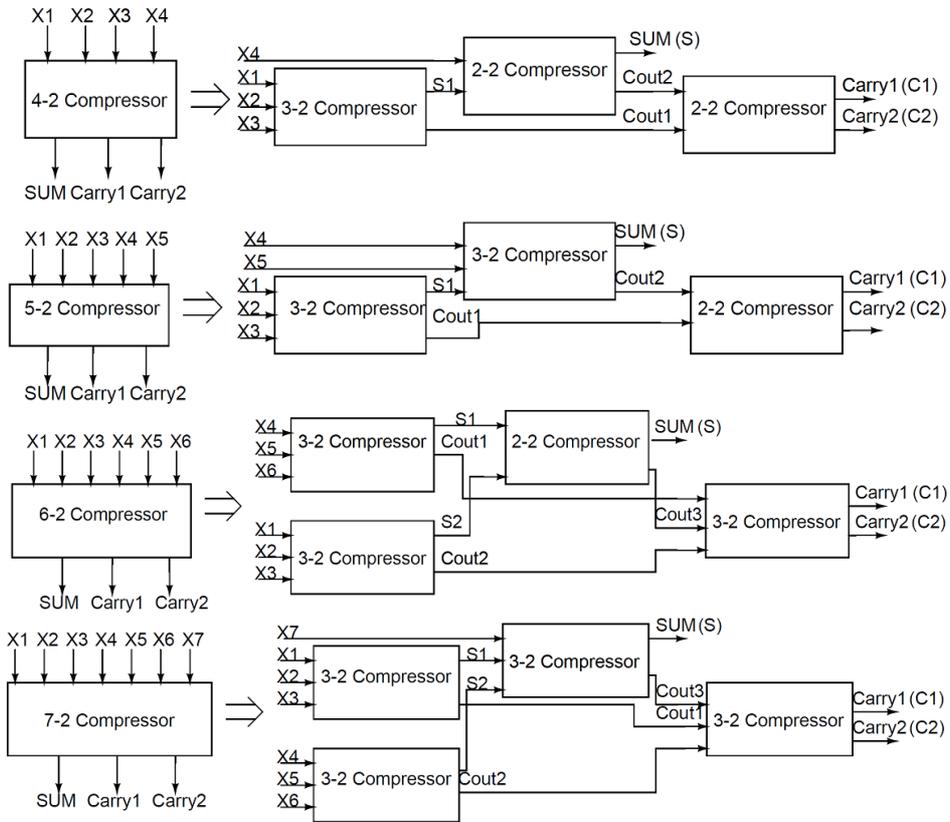
Fig. 7. The proposed designs of 4-2, 5-2, 6-2 and 7-2 compressors

In the Fig. 7, the primary inputs are shown as X1, X2, X3 ……… X7 and the primary outputs are Sum 'S', Carry1 'C1' and Carry2 'C2' respectively. These carry bits propagate to the next level of compressor as input bits. The compressors have been designed in such a way that they do not require a carry input from any of the adjacent compressor modules.

Simulation Results for Basic Modules of Compressors

All the basic modules and compressors of the referenced architectures, as cited in Table 3. The designed was performed in Cadence virtuoso EDA tool using 45 nm Technology libraries at Typical (TT) conditions.

All modules are simulated at 0.4 V supply voltage to obtain their results for sub-threshold operation. Table 2 shows the results of referenced architectures in terms of Power, Delay and PDP. Table 3 to 5 give the measured power, delay and PDP of the proposed basic modules for supply voltage varying from 0.3 to 0.5 V in steps of 0.5 V for sub-threshold operation. These results show that proposed modules function properly at supply voltage as low as 0.3 V.

The overall PDP results of the proposed compressor cells given in Table 6 are better than results of referenced architectures at 0.4 V supply voltage given in Table 3. The bar chart representations of results of proposed modules are shown in Fig. 8.

Table 2. Referenced designs at 0.4 V power supply using 45 nm technology

References	Module name	Power (nW)	Delay (ns)	PDP (Watt*sec 10^{-15})
Gupta *et al.* (2014)	AND gate	3.163	22.870	0.0913
Chang *et al.* (2004)	XOR gate	3.632	28.920	0.1050
Chang *et al.* (2004)	2:1 MUX	10.009	32.940	0.3296
Zimmermann and Fichtner (1997)	4:1 MUX	4.992	143.700	0.7176
Zimmermann and Fichtner (1997)	2-2 compressor	6.326	28.875	0.1824
Mahnoush *et al.* (2007)	3-2 compressor	43.780	71.586	0.7216
Karuna and Keshab (2001; Chang *et al.*, 2004)	4-2 compressor	18.485	127.700	2.3590
Karuna and Keshab (2001; Chang *et al.*, 2004)	5-2 compressor	25.550	187.210	4.7750
Weinan and Li (2008)	6-2 compressor	23.130	384.500	3.1120
Mahnoush *et al.* (2007)	7-2 compressor	43.780	235.900	10.3080

Table 3. Power comparison of basic modules

Power (nW) at 45 nm technology

Power supply basic modules	0.3 V	0.35V	0.4 V	0.45 V	0.5 V
4:1_MUX	1.6140	2.511	4.0990	7.101	12.990
2:1_MUX	1.0620	1.416	1.8460	2.367	2.994
AND/NAND gate	1.8553	2.479	3.2380	4.155	5.257
XOR gate	2.0570	2.747	3.5838	4.605	5.830
3-2 compressor	11.3280	30.686	81.4380	200.290	443.000
2-2 compressor	2.7700	3.694	4.8190	6.185	7.834
4-2 compressor	17.4920	38.906	92.1500	213.970	460.270
5-2 compressor	25.2300	64.399	165.7500	401.650	882.050
6-2 compressor	36.6170	95.151	247.2600	602.110	1325.000
7-2 compressor	44.9920	121.600	322.3700	792.150	1750.300

Table 4. Delay comparison of basic modules

Delay (ns) at 45 nm technology

Power supply basic modules	0.3 V	0.35 V	0.4 V	0.45 V	0.5 V
4:1_MUX	8.968	3.6070	1.5951	0.8049	0.4706
2:1_MUX	4.691	1.8530	0.8090	0.4100	0.2430
AND/NAND gate	5.841	2.2900	0.9986	0.5065	0.3003
XOR gate	7.592	2.9867	1.3045	4.1593	0.3883
3-2 compressor	9.559	3.8470	1.7020	0.8600	0.5010
2-2 compressor	4.683	1.8500	0.8090	0.4080	0.2420
4-2 compressor	14.291	6.7480	2.9538	1.4888	0.8703
5-2 compressor	19.505	7.8088	3.4357	1.7277	1.0000
6-2 compressor	24.885	9.9225	4.3586	2.1945	1.2761
7-2 compressor	20.591	8.2420	3.6339	3.6700	1.0689

Table 5. PDP comparison of basic modules

Power supply basic modules	0.3 V	0.35 V	0.4 V	0.45 V	0.5 V
4:1_MUX	0.014440	0.0090570	0.0065395	0.0057155	0.0061137
2:1_MUX	0.004984	0.0026240	0.0014940	0.0009720	0.0007270
AND/NAND gate	0.010830	0.0056780	0.0032337	0.0021040	0.0015780
XOR gate	0.015616	0.0082044	0.0046750	0.0191530	0.0022639
3-2 compressor	1.082000	0.1800000	0.1380000	0.1720000	0.2220000
2-2 compressor	0.009538	0.0050250	0.0028660	0.0018550	0.0013960
4-2 compressor	0.249900	0.2625000	0.2721000	0.3184000	0.4006000
5-2 compressor	0.492130	0.5028000	0.5694700	0.6940000	0.8827900
6-2 compressor	0.911200	0.9441000	1.0777000	1.3210000	1.6908000
7-2 compressor	0.926400	1.0023000	1.1714000	2.9072000	1.8709000
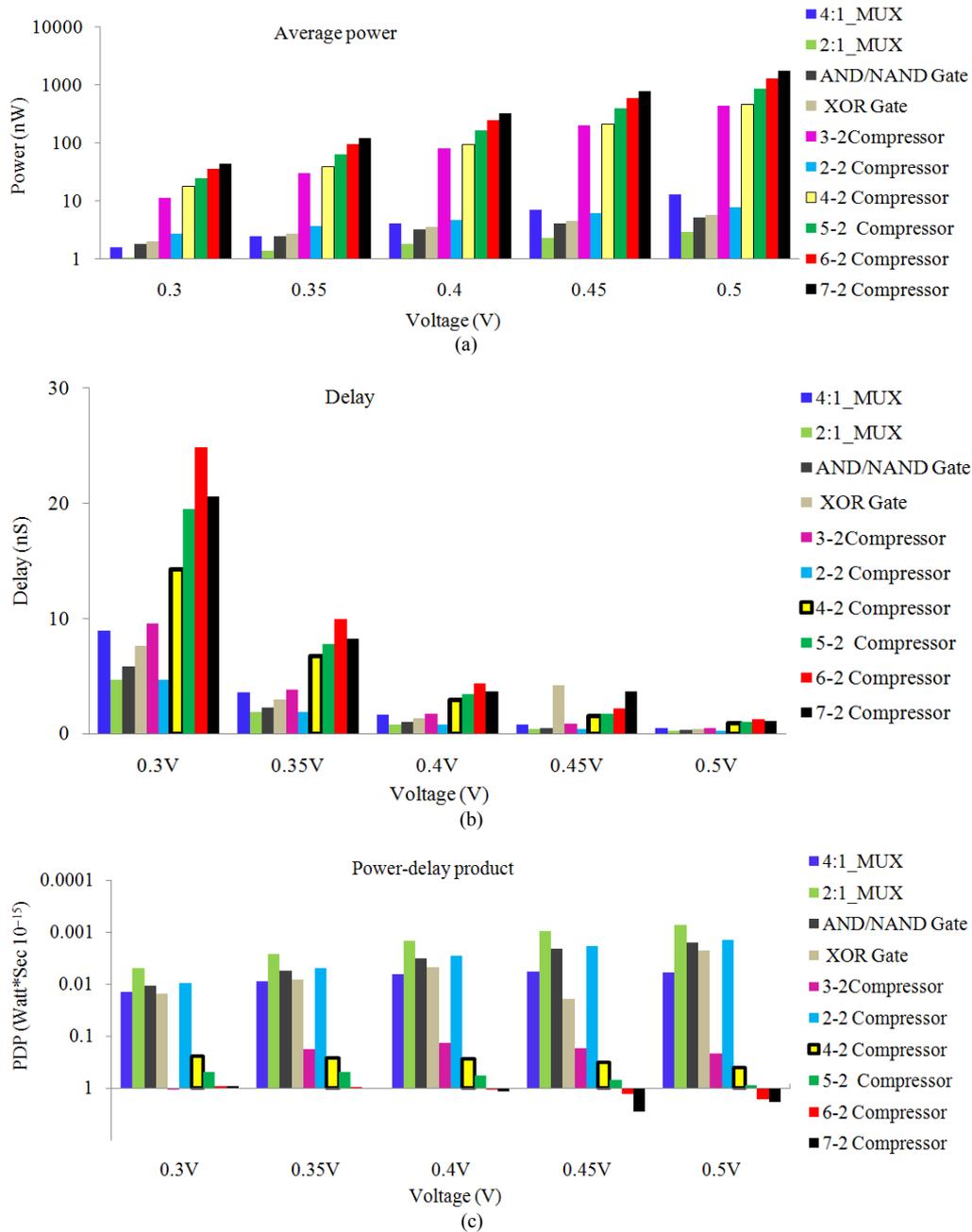
Fig. 8. Bar diagrams of basic modules (a) Power (b) Delay (c) Power-delay product

DADDA and Wallace Multipliers

Two of the most well-known column compression multipliers have been presented by Wallace and Dadda. Both architectures are similar with the difference occurring in the procedure of reduction of the partial products and the size of the final adder. In Wallace's scheme, the partial products are reduced as soon as possible but Dadda's method does minimum reduction necessary at each level. The size of final adder in Wallace multiplier is also slightly smaller as compared to the adder in Dadda multiplier. All the basic standard cells are same in both 4×4-bit and 8×8-bit of column compression Wallace and Dadda multipliers.

The Block diagram of $n * n$ bit column compression multipliers (Wallace and Dadda) using compressors is shown in Fig. 9.

These multipliers are composed of three modules:

- Partial product generate module
- Lower level compressors (2-2 and 3-2) and higher-level compressors (4-2, 5-2, 6-2 and 7-2) to reduce the partial products matrix to an addition of only two operands
- An HC adder for the final computation of the binary results

Partial Product Generate (PPG)

Conventionally, in the Wallace and Dadda multipliers the partial products are re-arranged in a reverse pyramid style. The PPG module is used to implement column compression for both Wallace and Dadda multipliers.

The proposed PPG module consists of bunch of MUX based AND gates, where each AND gate is implemented using 2:1 MUX as shown in Fig. 10.

The performance metrics considered for the proposed PPG modules are power, delay and PDP. To see the overall effects of these metrics, the proposed circuits are simulated at various supply voltages, ranging from 0.3 to 0.5 V as shown in Table 6.
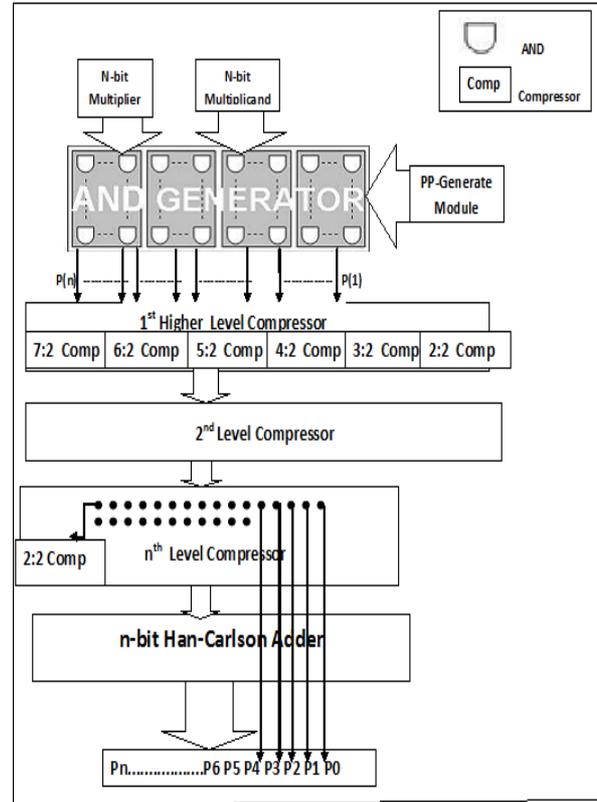
Fig. 9. Block diagram of n×n bit column compression multiplier
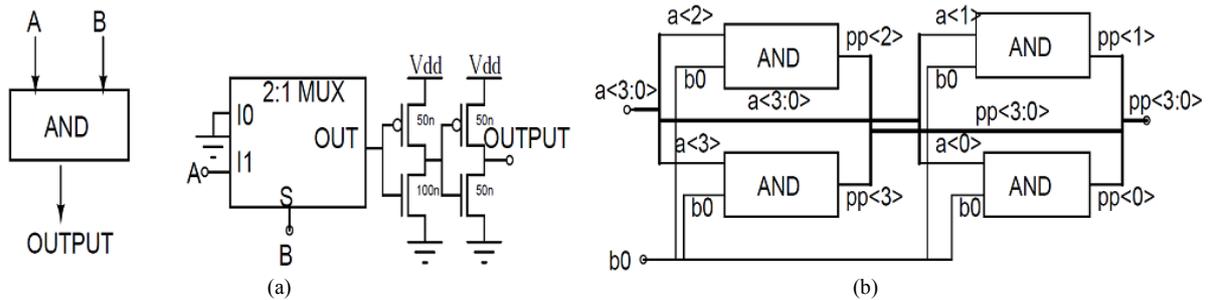
Fig. 10. Proposed module (a) and gate (b) Partial product generate module for Wallace and Dadda multiplier

Table 6. PPG Module at 45 nm technology for both Wallace and Dadda multiplier

	Power supply module name	0.3V	0.35V	0.4V	0.45V	0.5V
Power (nW)	4×4-bit Multiplier	7.421400	9.9180000	12.950000	16.6200000	21.0280000
	8×8-bit Multiplier	14.842000	19.8360000	25.905000	33.2410000	42.0570000
Delay (ns)	4×4-bit Multiplier	5.841000	2.2870000	0.998000	0.5060000	0.3000000
	8×8-bit Multiplier	5.841300	2.2908000	0.998700	0.5065000	0.3003000
PDP (Watt*Sec 10^{-15})	4×4-bit Multiplier	0.043350	0.0226800	0.012930	0.0084180	0.0063140
	8×8-bit Multiplier	0.086697	0.0454413	0.025872	0.0168385	0.0126297

Column Compression Technique for Dadda Multiplier

The arrangement of the partial products and the reduction stages for an 8×8-bit Dadda multiplier is shown in Fig. 11. The dots represent the partial products. The partial product matrix is reduced to a height of two using the column compression procedure developed by Dadda. The algorithm for iterative procedure is as follows:

- Assuming the minimum column height i.e., $h_1 = 2$ and calculating remaining column height using formula $h_{j+1} = floor (1.5*h_j)$ for increasing values of j. Continue this until the largest j is reached such that maximum column height for the multiplier to be designed is attained. Using this equation we get $h_1 = 2$, $h_2 = 3$, $h_3 = 4$, $h_4 = 6$, $h_5 = 9$ and so on. For example, in the first stage of the 8×8-bit Dadda multiplication shown in Fig. 11a, the maximum height of columns is 8, therefore, the value of h_j is 6, meaning that heights of the columns are reduced to a maximum of 6. Similarly in the second stage, shown in Fig. 11b, the maximum height of column is 6 and value of h_j is 4, meaning that heights of the columns are reduced to a maximum of 4
- All the columns, with heights greater than h_j, are reduced to a height of h_j using higher level compressors of different sizes. If the column height has to be reduced by one, use a 2-2 compressor else use a 3-2 compressor. A 4-2 compressor is used if the height has to be reduced by 3, a 5-2 compressor is used if it has to be reduced by 4 and so on and continue this step till the column height is reduced to h_j
- The iterations continue until two elements remain in each queue. Once such a state has been reached then the reduction phase is completed and then it can be fed to the final adder
- The first element of all queues form the first input to the adder and the second element forms the second input to the adder. Energy efficient HC adder is used for the final summation of the 4×4-bit and 8×8-bit Wallace and Dadda multipliers
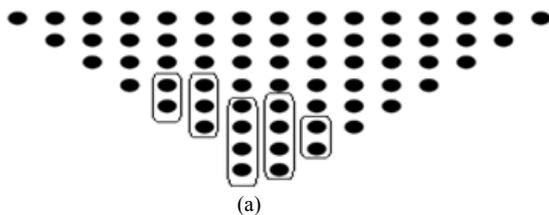
Column compression scheme and final computation using HC adder for 4×4-bit Dadda multiplier is shown in Fig. 12.

Column Compression Technique for Wallace Multiplier

The arrangement of the partial products and the reduction stages for an 8×8-bit Wallace multiplier is shown in Fig. 13. The dots represent the partial products.

The algorithm for iterative procedure for reduction of column compression matrix to a height of 2 using higher-level compressors is described below:

- Find out the maximum height of columns in the dot matrix array. If it is greater than 2, reduce the height by following the recursive procedure described below
- Check the height of each column. If it is 1, no reduction is done. If it is 2, use a 2-2 compressor. Use 3-2 compressor, 4-2 compressor, 5-2 compressor and 6-2 compressor if the height of the column is 3, 4, 5 and 6 respectively else use a 7-2 compressor and check the height of column again. Continue the reduction till the height of column becomes ≤1
- Repeat the above step for all other columns and at the end, en-queue the 'sum' strings of all the counters into the same queues. The only carry in case of 2-2 and 3-2 compressors are en-queued into the next queue. In case of 4-2, 5-2, 6-2 and 7-2 compressors, the carry Carry1 is en-queued into the next queue and the carry Carry2 is en-queued into the queue following it
- Again find out the maximum height of columns and continue the reduction using the above recursive procedure till maximum height reaches 2
- Stop the reduction if the height of the matrix becomes two, after which it can be fed to final adder. Once such a state has been reached then the reduction phase is completed
- Once the height of matrix is reduced to two, an adder is used to generate the final product

Column compression scheme and final computation using HC adder for 4×4-bit Wallace multiplier is shown in Fig. 14.

(a)

(b)

(c)

(d)

(e)
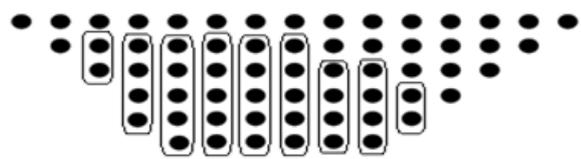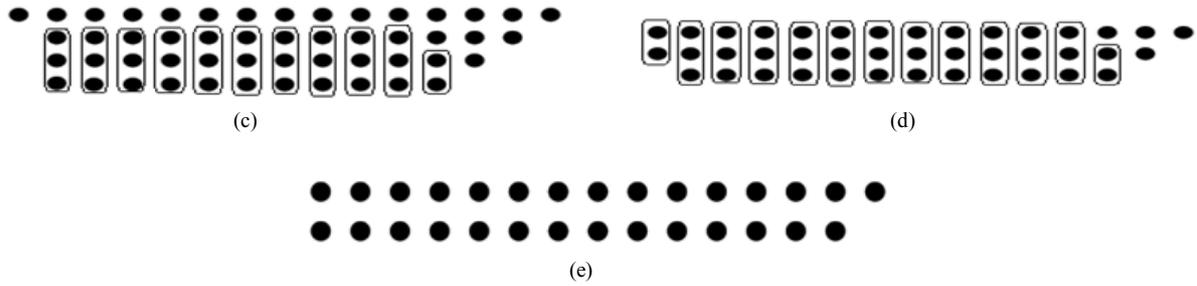
Fig. 11. Column compression scheme for 8×8-bit Dadda multiplier using higher order compressors
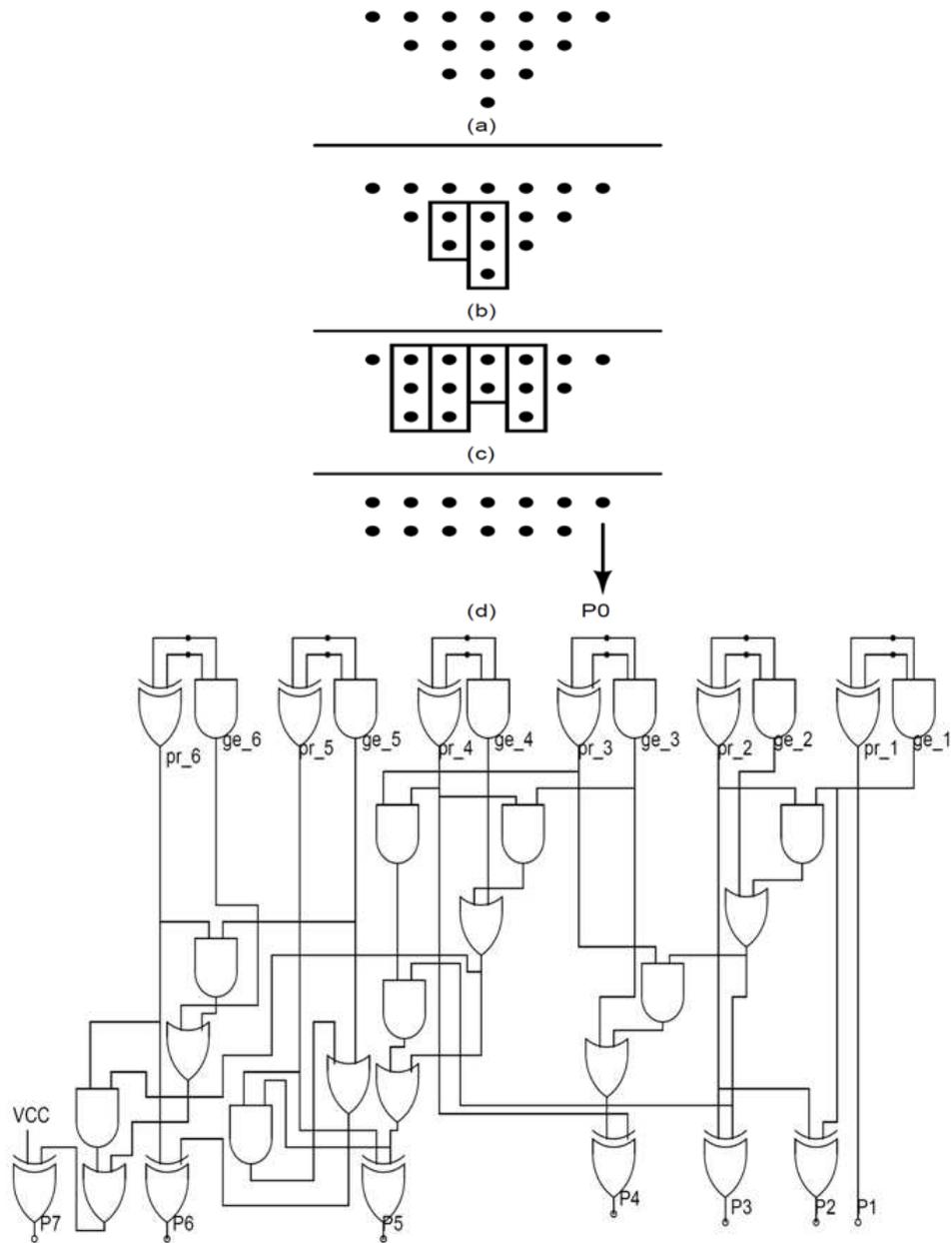
Fig. 12. Column compression scheme and final computation using HC adder for 4×4-bit Dadda multiplier
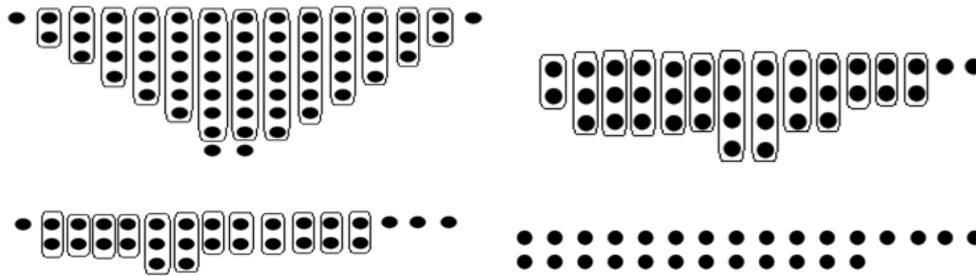
Fig. 13. Column compression scheme for 8×8-bit Wallace multiplier using higher order compressors
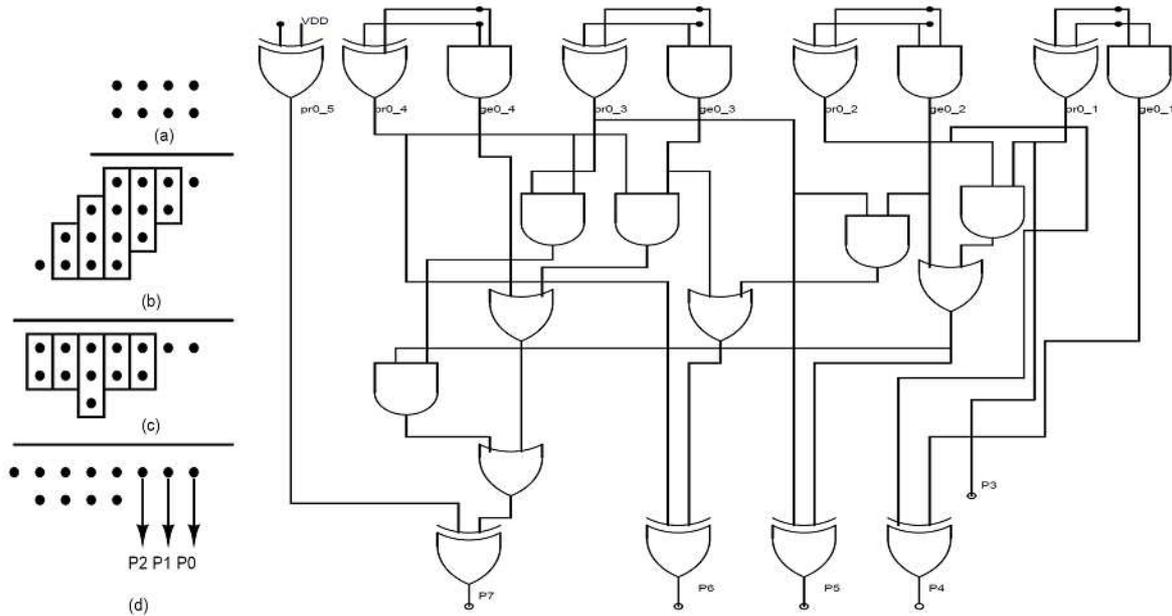
Fig. 14. Column compression scheme and final computation using HC adder for 4×4-bit Wallace multiplier

Simulation Results for Dadda and Wallace multiplier

A parametric analysis on varying the PMOS transistor width was done to observe the power consumption. The power consumption is least when we have minimum size for both NMOS and PMOS. As per the conceptual analysis to allow the same current in both PMOS and NMOS, the W/L ratios of PMOS and NMOS should be in the inverse ratio of the mobility ratios of hole to electron. So to have a symmetrical design, the W/L ratios of PMOS and NMOS are taken in the ratio 2. The complete ASIC implementation of the proposed 4×4-bit and 8×8-bit of Wallace and Dadda design is also done using the Cadence design flow. The proposed design has been developed using Verilog-HDL and synthesized in Encounter RTL compiler using typical libraries of 45 nm technology at nominal supply voltage (0.7 V) using semi-custom design technique. The test bench is created for simulation and logic verification by NCSIM simulator. The Cadence SoC Encounter is used for Placement & Routing (P&R). Parasitic extraction is performed using Encounter Native RC extraction tool. The extracted parasitic RC (SPEF format) is back annotated to Common Timing Engine in Encounter Platform for static timing analysis. ASIC implementation results before and after post-layout simulation using semi custom design techniques are shown in Table 7.

Table 8 show results of full custom designs of 4×4-bit and 8×8-bit Wallace and Dadda multipliers in sub-threshold regime. The performance parameters are power, delay and PDP. To see the overall effects of varying supply voltage on these parameters, the circuits are simulated at voltage ranging from 0.3 to 0.5 V in steps of 0.5 V. It is verified that the circuits are functional at slow-slow and fast-fast corners also. Since the delay of the designed multiplier circuit is proportional to the logarithm of the number of bits in the multiplier and the delay of its building blocks, so to measure the critical path delay and to verify the

functionality of multipliers, n-numbers of test patterns have been applied. The critical path delay has been found for the input combinations $\{a_{3-0} = 1111$ and $b_{3-0} = 1000\}$ for 4×4-bit Wallace and Dadda multipliers and $\{a_{7-0} = 11111111$ and $b_{7-0} = 00001000\}$ for 8x8-bit Wallace and Dadda multipliers.
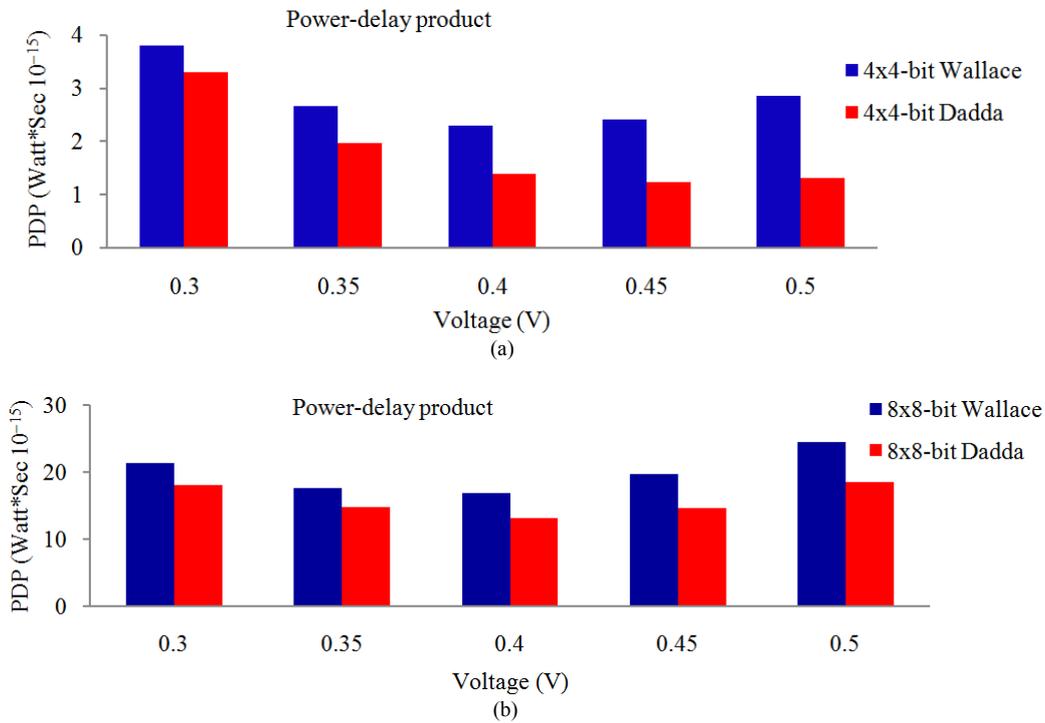
Fig. 15. PDP comparison graphs of Wallace and Dadda multipliers (a) 4×4-bit (b) 8×8-bit

Table 7. Multipliers using semi-custom design technique at nominal supply voltage

Module name	SOC results (Post layout)		
	Power (µW)	Delay (ns)	PDP (10^{-15})
4×4-bit Wallace multiplier	56.70	1.79812	101.9530
4×4-bit Dadda multiplier	50.48	1.69810	85.7200
8×8-bit Wallace multiplier	295.20	4.99510	1474.5500
8×8-bit Dadda multiplier	238.70	4.89510	1168.3300

Table 8. Multipliers using full custom design technique

Power supply voltage (V)	Power (µW)		Delay (ns)		PDP (Watt*sec 10^{-15})	
	Wallace	Dadda	Wallace	Dadda	Wallace	Dadda
(a) 4×4-bit Wallace and Dadda multipliers						
0.3	0.13530	0.12540	28.0700	26.3080	3.7978	3.2990
0.35	0.24180	0.19100	11.0460	10.3140	2.6709	1.9699
0.4	0.47810	0.31090	4.8203	4.4906	2.3045	1.3961
0.45	0.98780	0.54150	2.4386	2.2730	2.4088	1.2308
0.5	1.98800	0.97420	1.4387	1.3414	2.8601	1.3067
(b) 8×8 Wallace and Dadda multipliers						
0.3	0.74990	0.68013	28.4550	26.5810	21.3380	18.0780
0.35	1.56790	1.36740	11.1910	10.8420	17.5460	14.8250
0.4	3.45700	2.93920	4.8830	4.5040	16.8800	13.2380
0.45	7.98990	6.42360	2.4695	2.2906	19.7310	14.7130
0.5	16.84700	13.34500	1.4569	1.3916	24.5440	18.5700

Table 9. Comparison results of proposed and reference designs at 0.4V using 45 nm technology

		Power (µW)		Delay (ns)		PDP (Watt*sec 10^{-15})	
References	Module name	Conventional	Proposed	Conventional	Proposed	Conventional	Proposed
Dandapat *et al.* (2010)	4×4-bit Wallace	0.72340	0.4781	110.910	4.8203	80.23	2.3045
Naveen *et al.* (2014)	4×4-bit Dadda	0.56230	0.3109	81.721	4.4906	45.95	1.3961
Ramkumar *et al.* (2013)	8×8-bit Wallace	2.42300	3.4570	223.010	4.8830	540.35	16.8800
Manas *et al.* (2012)	8×8-bit Dadda	1.90100	2.9392	187.110	4.5040	355.60	13.2380

The 4×4-bit and 8×8-bit Wallace and Dadda multipliers of the referenced architectures, as cited in Table 9. are designed at 45 nm CMOS technology for 0.4 V supply voltage to obtain their results for sub-threshold operation. It shows comparative simulation results of the proposed design with the referenced architectures, which used conventional design of compressor blocks to implement the multiplier architectures in sub-threshold regime.

The designed multipliers using proposed compressors show an overall reduction in PDP as compared to conventional multiplier architectures and give best results at 0.4 V power supply. In addition, it has been observed that the PDP improvement for Dadda multiplier is better than Wallace multiplier in sub-threshold regime. The graphical representations of PDP of both multipliers are shown in Fig. 15.

Conclusion

The compressors are the basic building blocks in the column compression multipliers and hold the key for minimizing the power consumption of the overall circuit, Therefore, selecting an appropriate compressor cells can significantly improve the overall multiplication computations. The use of compressors in the multipliers reduces the overall PDP due to less number of stage operations. The main focus of this paper was to optimize overall PDP of multiplexers based compressors using TG logic family in subthreshold regime. The proposed library of power efficient compressors have been used in the design of low-power 4×4-bit and 8×8-bit Wallace and Dadda multipliers at 45 nm technology at power supply voltages, ranging from 0.3 to 0.5 V. The result show on an average 89% and 96.8% improvement in the PDP for proposed compressor blocks and multipliers at supply voltage of 0.4V, when compared with the referenced designs. The future scope includes verifying the results for larger operand size multipliers.

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Author's Contributions

Priya Gupta: Made considerable contributions to design, analysis and interpretation of the proposed design of multipliers. Contributed in all experiments, research plan, data-analysis and writing of manuscript.

Anu Gupta: Made considerable contributions to conception and design. Analysis of multiplier operation, verifying multiplier's design, contributed in reviewing the article. Give final approval of the version to be submitted and any revised version.

Abhijit Asati: Contributed in reviewing the article critically for significant intellectual content. Give final approval of the version to be submitted and any revised version.

Ethics

This article is original and contains unpublished material. The corresponding author confirms that all of the other authors have read and approved the manuscript and no ethical issues involved.

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